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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
HO, TU TU V	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 07/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/816,282	CHANG, PETER L.D.	
	Examiner	Art Unit	
	Tu-Tu Ho	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 June 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) *11-16 and 23-28* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4-10 and 17-20* is/are rejected.

7)☒ Claim(s) *3,21 and 22* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/01/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Oath/Declaration

1. The oath/declaration filed on 08/09/2004 is acceptable.

Election/ Restriction

2. Applicant's election of Invention II, claims 1-10 and 17-22, in the reply filed on 06/22/2005 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

3. Claims 11-16 and 23-28 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention, there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on 06/22/2005, as noted above.

Claim Rejections § 102 & § 103

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in
(1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or
(2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall

have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

The following is a quotation of 35 U.S.C. §103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. **Claims 1-2, 6-8, 17, and 20 are** rejected under 35 U.S.C. 102(e) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Mathew et al. U.S. Patent 6,831,310 (the '310 reference).

The '310 reference discloses in Figs. 11-12 and respective portions of the specification a method of fabricating a memory device and the device thereof as claimed or substantially as claimed. In particular, the reference discloses a memory device having a FinFET transistor with three independently controlled gates, each could independently control a conduction characteristic of the transistor or independently store charge as a volatile or a nonvolatile memory function (columns 7 and 8, particularly, "Such contacts could be used to implement additional biasing of the channels 113 and 114, the layer of nanoclusters of charge storage layer 143 and the layer of nanoclusters of charge storage elements 144 or charge storage layer 118 and charge storage layer 120", column 7, lines 44+).

More particular and in reference to **claims 1 and 17**, the reference discloses a memory device and a method of fabricating thereof, comprising:

a plurality of parallel, spaced-apart silicon lines (generally defined by 113, 111) disposed on an oxide layer (109); and

a plurality of parallel, spaced-apart conductive lines (generally defined by 153,155,157,159, only one line being shown), generally perpendicular to the silicon lines disposed on the oxide layer, the conductive lines being non-continuous at intersections of the silicon lines, each intersection forming a body region (113, 111, also known as channel region, as it is sandwiched by source and drain regions, which are shown in the figures as being covered by source and drain contacts 179,181; or 113/143, 111/144) in the silicon line and a first gate (153) and a second gate (155) on opposite sides of the body region formed from the conductive lines, the gate being insulated from the body regions;

However, the reference fails to teaches that the first gates are coupled to word lines in the memory, that the second gates are coupled for biasing the body regions (in re claim 1), and that the drain regions are connected to bit lines (in re claim 17).

Nevertheless, as for the limitation "the first gates being coupled to word lines in the memory", as mentioned above, the reference teaches that "[S]uch contacts [to the gates] could be used to implement additional biasing of the channels 113 and 114, the layer of nanoclusters of charge storage layer 143 and the layer of nanoclusters of charge storage elements 144 or charge storage layer 118 and charge storage layer 120", and in the art that means connecting one of the gates to the word line in the memory device (see, for example, Iwata et al., U.S. Patent Application Publication 20020114191, Figs. 68-92).

As for the limitation "the second gates being coupled for biasing the body regions", as mentioned above, the reference teaches that "[S]uch contacts [to the gates] could be used to implement additional biasing of the channels 113 and 114, the layer of nanoclusters of charge

storage layer 143 and the layer of nanoclusters of charge storage elements 144 or charge storage layer 118 and charge storage layer 120", with channels, as mentioned above, are body regions.

As for the limitation "connecting the drain regions to bit lines, although not disclosed, connecting the drain regions to the bit lines is how memory devices having drain regions are controlled. See, for example, Iwata et al., U.S. Patent Application Publication 20020114191, Figs. 68-92).

Referring to **claim 2**, although not explicitly disclosed, doping the body regions (channel regions) with a first conductivity type dopant and doping the source and drain regions with a second conductivity type dopant is how one of ordinary skill in the art would do to form the device including a body region (channel region), the drain region, and the source region, which device is otherwise known as a transistor, or specifically in the instant case, a FinFET).

Referring to **claims 6 and 20**, the reference further discloses that the conductive lines (147 that forms the gates 153,155,157,159) comprise polysilicon (column 6, lines 30+).

Referring to **claim 7**, the reference further discloses that the spacers (such as 135,145) are disposed along vertical sides of the conductive lines.

Referring to **claim 8**, the reference further discloses that peripheral circuits (such as 105, Fig. 14) formed on a common substrate with the memory, with substrate being interpreted broadly.

Claim Rejections - 35 USC § 103

5. **Claims 4-5** are rejected under 35 U.S.C. §103(a) as being unpatentable over Mathew et al. U.S. Patent 6,831,310 (the '310 reference) as applied above and further in view of Madurawe U.S. Patent Application Publication 20040152245.

The '310 reference discloses a memory device including a transistor as claimed and as detailed above but fails to teach that the source regions are coupled to ground potential and that the biasing of the body regions by the second gates comprises coupling the second gates to a negative potential.

Madurawe, in also disclosing a transistor having a source region and a body region, teaches that in controlling the transistor, the source region should be coupled to a ground potential and the body to a negative potential to ensure complete turn-off of the transistor (paragraphs [0006]-[0008]).

Therefore, it would have been obvious to one of ordinary skill in the art the time the invention was made to form the reference's transistor such that the source regions are coupled to ground potential and that the biasing of the body regions by the second gates comprises coupling the second gates to a negative potential. One would have been motivated to make such a change in view of the teachings in Madurawe that such an annragement ensure complete turn-off of the transistor.

6. **Claim 9** is rejected under 35 U.S.C. §103(a) as being unpatentable over Mathew et al. U.S. Patent 6,831,310 (the '310 reference).

The '310 reference discloses a memory device including a transistor as claimed and as detailed above but fails to teach that the first conductivity type is p type and the second

conductivity type is n type. However, selecting the first conductivity type a p-type among n and p types and selecting the second conductivity type an n-type among n and p types are within the ability of a person of ordinary skill in the art, therefore would have been obvious.

7. **Claim 10** is rejected under 35 U.S.C. §103(a) as being unpatentable over Mathew et al. U.S. Patent 6,831,310 (the '310 reference) as applied above and further in view of Van Houdt et al. U.S. Patent 6,243,293 and in view of Nakagawa 6,137,134.

The '310 reference discloses a memory device as claimed and as detailed above including body regions (113/143, 111/144) each providing a storage for charge (from element 143 or 144) for a memory cell but fails to teach that adjacent memory cells share source regions, drain regions, first gates and second gates.

Van Houdt et al. and Nakagawa, also in disclosing a memory device, teaches respectively that adjacent memory cells sharing bitline contacts and gate helps reduce memory device area (column 6, lines 33-45 and column 12, lines 50-67) and that adjacent memory cells sharing source and drain regions also helps reducing memory size and increasing speed (column 2, lines 25-45, column 3, lines 23-35).

Therefore, it would have been obvious to one of ordinary skill in the art the time the invention was made to form the reference's memory device such that adjacent memory cells share source regions, drain regions, first gates and second gates. One would have been motivated to make such a change in view of the teachings in Van Houdt et al. and Nakagawa that such configuration saves memory space.

8. **Claims 18 and 19** are rejected under 35 U.S.C. §103(a) as being unpatentable over Mathew et al. U.S. Patent 6,831,310 (the '310 reference) as applied above and further in view of Lin et al. U.S. Patent 6,190,981.

The '310 reference discloses a method of fabricating a memory device including a transistor as claimed and as detailed above but fails to teach that formation of the source and drain regions is by implanting twice. Specifically, the reference fails to teach that the formation of the source and drain regions comprises implanting the source and drain regions with a first conductivity type dopant, forming spacers on the sides of the conductive lines and again, doping the source and drain regions with the first conductivity type dopant such that the spacers block portions of the source and drain regions. Nevertheless, the claimed process, which is known as LDD or halo doping, is known in the art to reduce the so-called short channel effect for the transistor.

For example, Lin et al. U.S. Patent 6,190,981, in also disclosing a transistor, teaches that by forming a LDD doping (Figs. 3A-3F), the occurrence of the short channel effect is decreased (column 4, lines 35-45).

Therefore, it would have been obvious to one of ordinary skill in the art the time the invention was made to form the reference's source and drain regions with a LDD process. One would have been motivated to make such a change in view of knowledge in the art as disclosed by Lin that the process - formation of the source and drain regions by implanting the source and drain regions with a first conductivity type dopant, forming spacers on the sides of the conductive lines and again, doping the source and drain regions with the first conductivity type

dopant such that the spacers block portions of the source and drain regions - decreases occurrence of the short channel effect.

Referring to claim 19, Lin further discloses the formation of a salicide (316b, Fig. 3E) on the source and drain regions thus formed, and although not taught, salicide formation is to reduce contact electrical resistance as is also known in the art.

Allowable Subject Matter

9. Claims 3 and 21 and dependent-upon-claim-21 claim 22 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is an examiner's statement of reasons for the indication of allowable subject matter: The cited art, whether taken singularly or in combination, especially when all limitations are considered within the claimed specific combination, fails to teach or render obvious a method of fabricating a memory device and the device thereof including all exclusive limitations as recited in claims 3 and 21, comprising word lines; and body regions on an oxide layer formed by intersecting parallel silicon lines with parallel discontinuous conductive lines at generally perpendicular angles; the discontinuity formed at the intersections; the body regions formed from the silicon lines; first gates and second gates formed on opposite sides of and isolated from each of the body regions and formed from the discontinuous conductive lines; the first gates being coupled to the word lines; each pair of the second gates being connected together by a respective overlying metal bridge; and either that the second gates being coupled for biasing the body regions; or that the device further comprises source and drain regions on

either side of each of the body regions, the drain regions being connected to bit lines of the memory device.

Conclusion

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tu-Tu Ho whose telephone number is (571) 272-1778. The examiner can normally be reached on 6:30 am - 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, DAVID NELMS can be reached on (571) 272-1787. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TH

Tu-Tu Ho
July 01, 2005